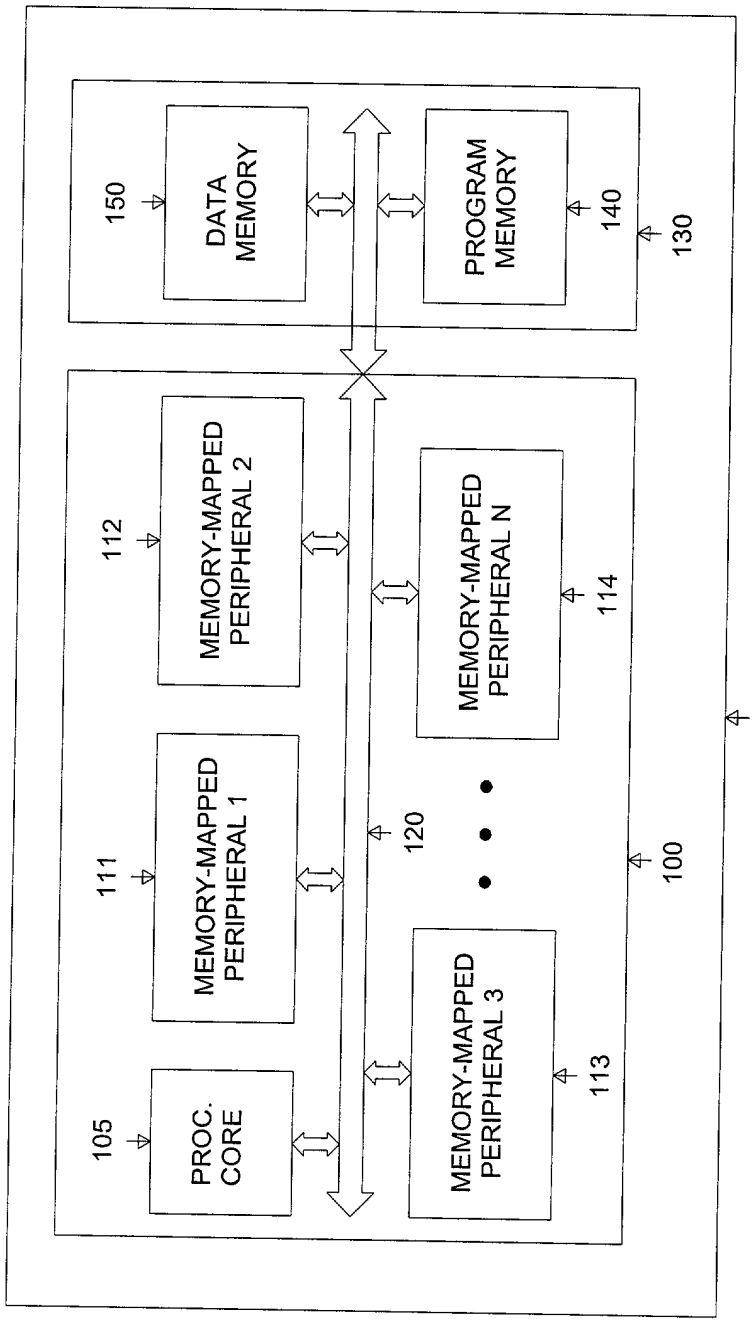
10
100
105
PROC. CORE
111
MEMORY-MAPPED PERIPHERAL 1
112
MEMORY-MAPPED PERIPHERAL 2
113
MEMORY-MAPPED PERIPHERAL 3
114
MEMORY-MAPPED PERIPHERAL N
120
130
140
PROGRAM MEMORY
150
DATA MEMORY

FIGURE 1

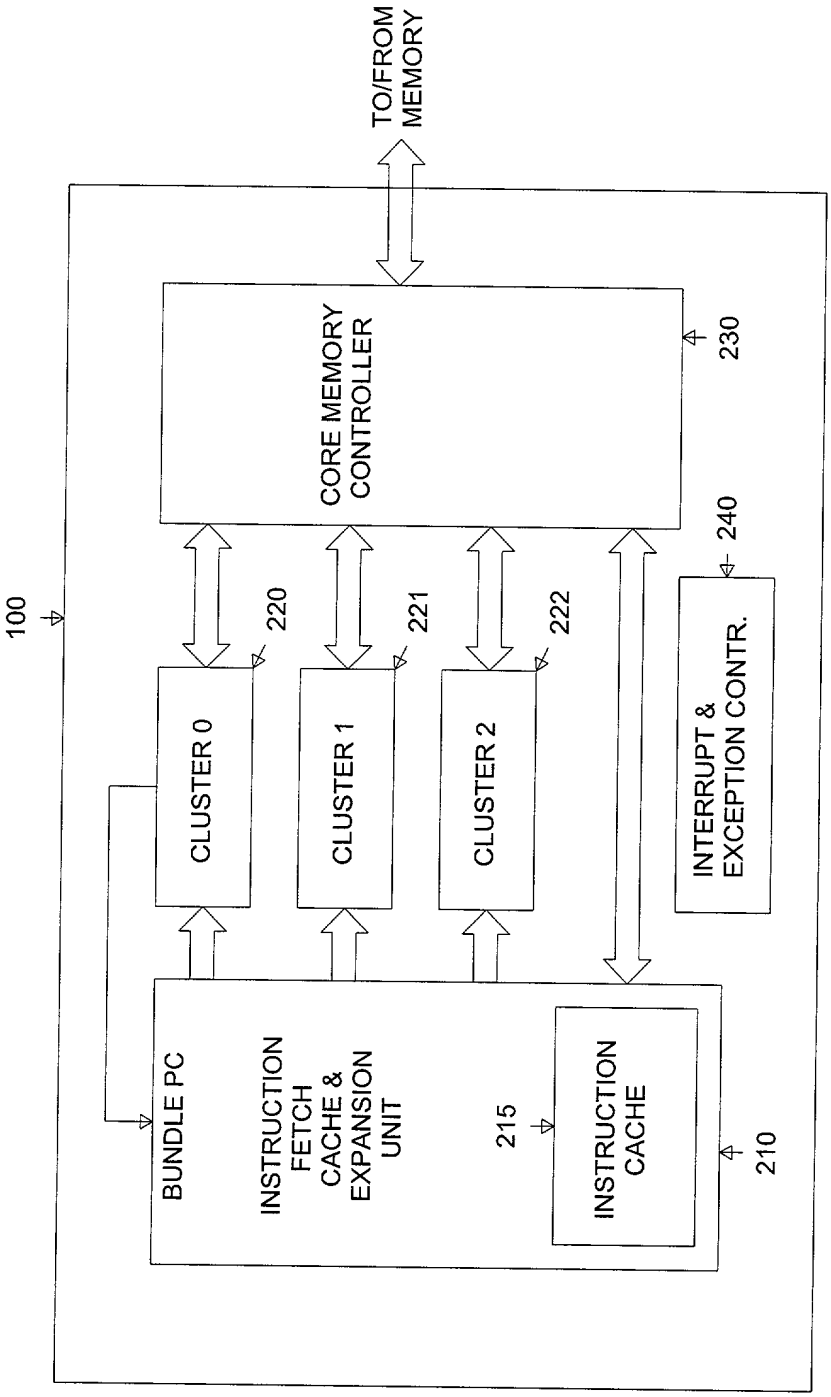
TO/FROM MEMORY
CORE MEMORY CONTROLLER
230
100
220
221
222
240
CLUSTER 0
CLUSTER 1
CLUSTER 2
INTERRUPT & EXCEPTION CONTR.
BUNDLE PC
INSTRUCTION FETCH CACHE & EXPANSION UNIT
215
INSTRUCTION CACHE
210

FIGURE 2

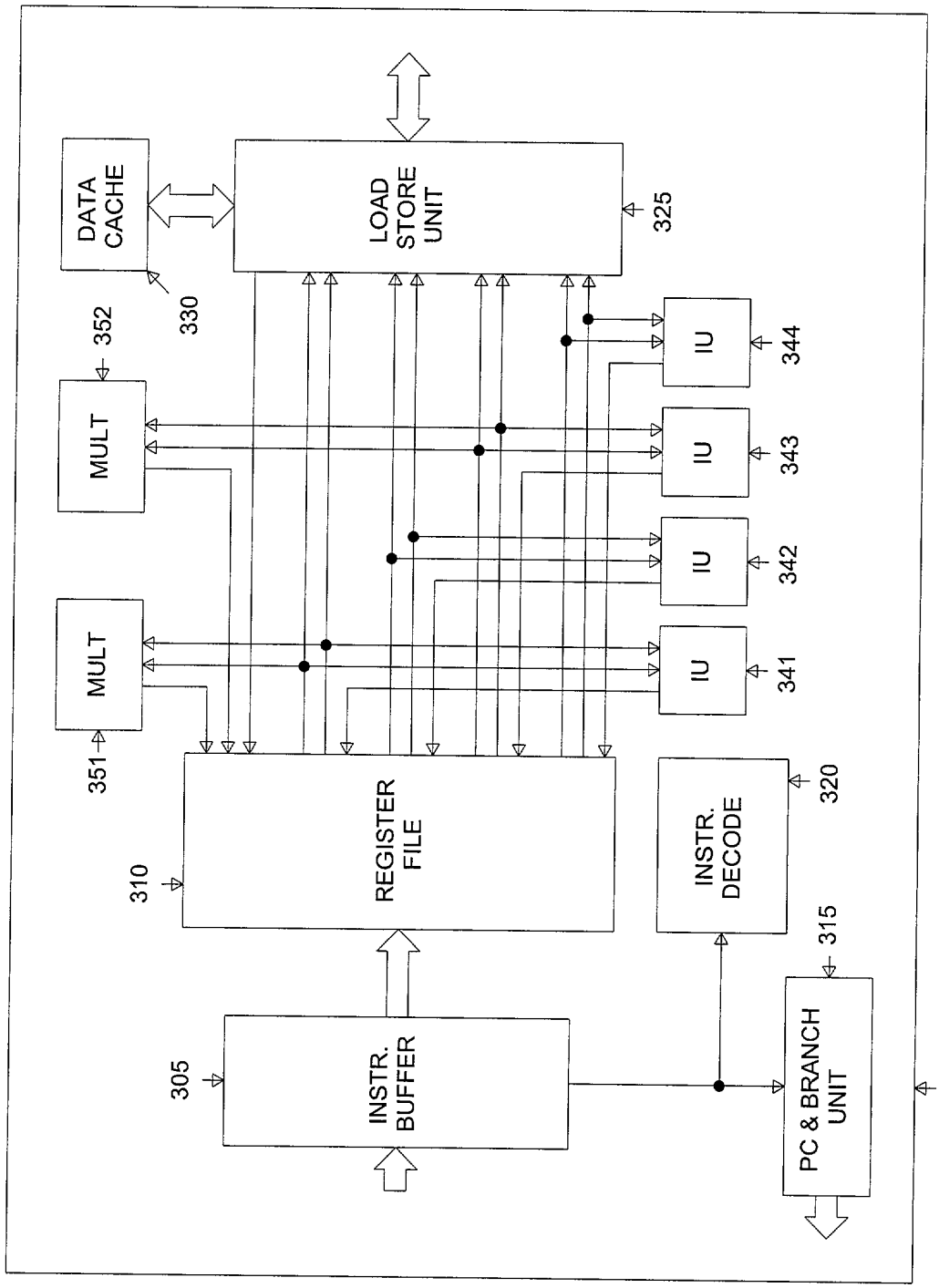
DATA CACHE
330
LOAD STORE UNIT
325
352
MULT
MULT
351
IU
344
IU
343
IU
342
IU
341
REGISTER FILE
310
INSTR. DECODE
320
315
INSTR. BUFFER
305
PC & BRANCH UNIT
220

FIGURE 3

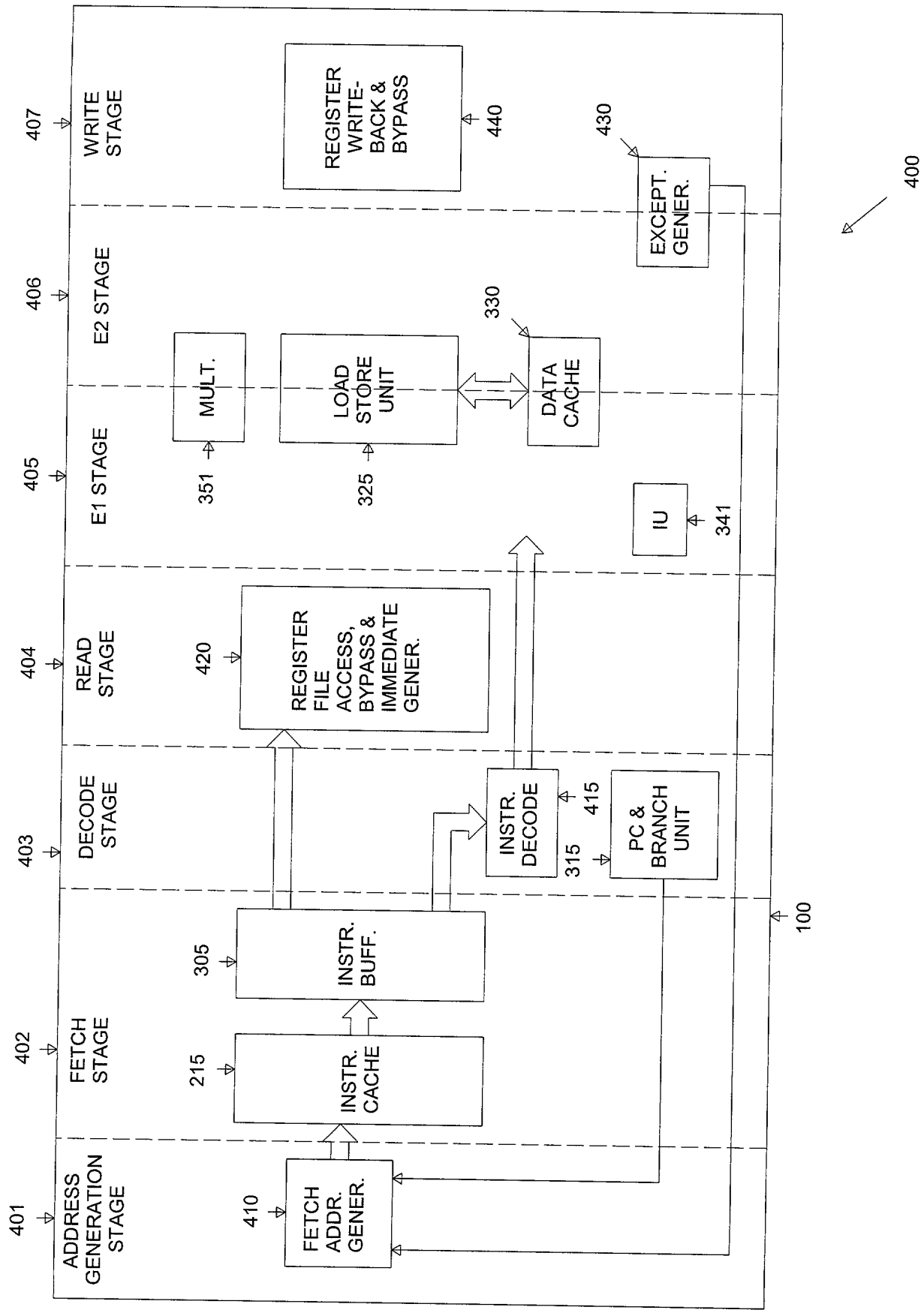
ADDRESS GENERATION STAGE
401
FETCH STAGE
402
DECODE STAGE
403
READ STAGE
404
E1 STAGE
405
E2 STAGE
406
WRITE STAGE
407
FETCH ADDR. GENER.
410
INSTR. CACHE
215
INSTR. BUFF.
305
INSTR. DECODE
315
PC & BRANCH UNIT
415
REGISTER FILE ACCESS, BYPASS & IMMEDIATE GENER.
420
MULT.
351
LOAD STORE UNIT
325
DATA CACHE
330
IU
341
EXCEPT. GENER.
430
REGISTER WRITE-BACK & BYPASS
440
100
400

FIGURE 4

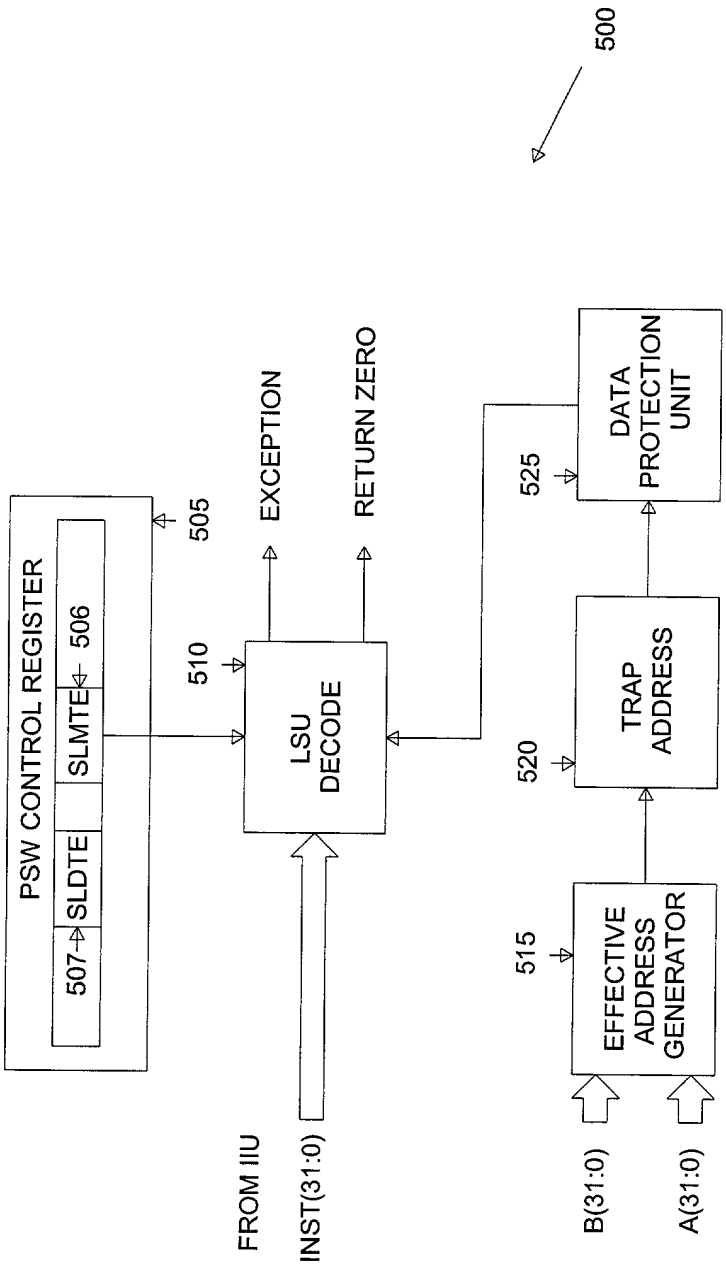
500
PSW CONTROL REGISTER
507
SLDTE
SLMTE
506
505
510
LSU DECODE
EXCEPTION
RETURN ZERO
525
DATA PROTECTION UNIT
520
TRAP ADDRESS
515
EFFECTIVE ADDRESS GENERATOR
FROM IIU
INST(31:0)
B(31:0)
A(31:0)

FIGURE 5

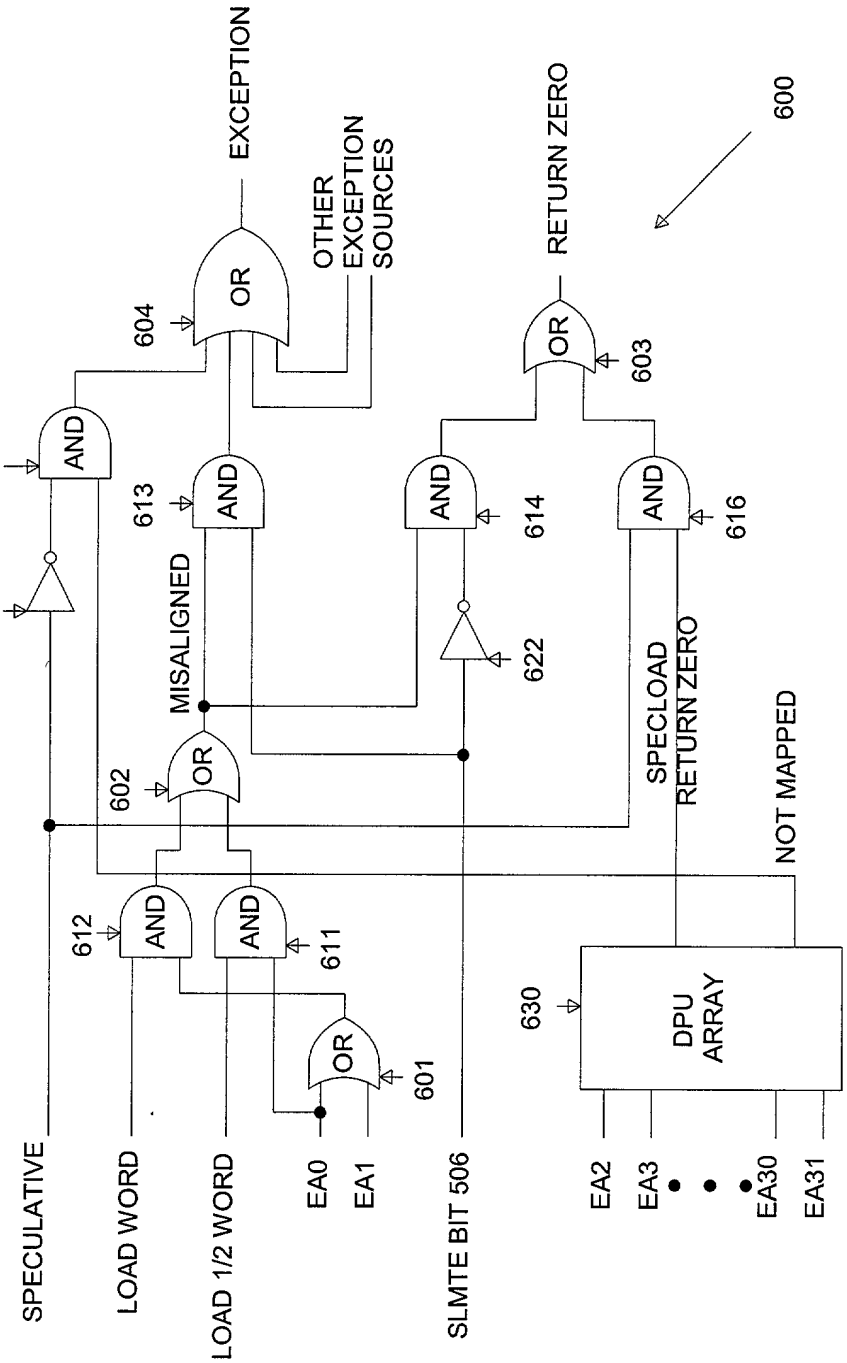
600
EXCEPTION
OTHER EXCEPTION SOURCES
RETURN ZERO
604
OR
603
OR
615
AND
613
AND
614
AND
616
AND
621
622
MISALIGNED
602
OR
SPECLOAD RETURN ZERO
NOT MAPPED
612
AND
611
AND
601
OR
630
DPU ARRAY
SPECULATIVE
LOAD WORD
LOAD 1/2 WORD
EA0
EA1
SLMTE BIT 506
EA2
EA3
EA30
EA31

FIGURE 6